3-D Camera SoPC Design Architecture

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Abstract— It is often seen that the available knowledge base within an organisation influences the selection of the design platform. The two major contenders for signal processing hardware platforms are DSP processor and FPGA. DSP processor offers high compute intensive complete embedded product where as FPGA offers high flexibility to a System on Programmable Chip (SoPC) designer for proof of concept at formative stage of the system design leading to manufacturable prototype at a later stage before the final ASIC implementation. The constraint aware design brings forth many challenges in terms of cost, size, memory, performance and time to market. The paper highlights the design cycle of finding the right platform after weighing the pros and cons of the design constraints and the design space exploration by way of a project based case study of a 3-D camera controller SoPC design on FPGA.

Index Terms— DSP, FPGA, SoPC, Camera, Embedded

1 INTRODUCTION

Electronics systems in general can be categorized into two major systems; i.e., Personal Computer Systems and the rest are the Embedded Systems. The hardware platforms for embedded systems design fall into three electronic device families namely Microcontroller, DSP processor and FPGA. There are combinations of these entities available from chip vendors to suit a particular application. Few examples are DSPIC from Microchip combines DSP and Microcontroller, Actel offers Microcontroller and FPGA combination, and Xilinx announced FPGA with ARM hard processor.

DSP processors have DSP specific instructions with floating or fixed point computing capabilities. However to provide digital logic functionalities like timing signal generation, an extra programmable logic device such as CPLD or FPGA is required. On the other hand FPGA, having ocean of gates, are like temples without god, where a domain as demigod need to be installed by System on Programmable Chip designers. Embedding a Soft processor in FPGA to handle microcontroller like functionality along with the resident DSP specific primitives of FPGA makes it the most versatile among the design platforms.

The paper presents platform independent top-level design architecture of a 3-D camera controller and highlights the selection process of possible architectures based on DSP only, FPGA only and a heterogeneous combination of DSP and FPGA. The choice of the final architecture led to FPGA, deviating from the DSP processor, in spite of DSP being the natural choice of a hardcore DSP company with immense in-house knowledgebase on DSP tools and technologies. The project outsourcing company, who intended to design an ASIC for the 3-D camera controller, influenced the selection of the design architecture and the world knows that the FPGAs are the best prototype Pre-ASIC design platform.

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The paper is organized as follows; 3-D camera system is introduced in Section 2, Section 3 covers System partitioning and architectures combination on DSP and FPGA. Section 4 covers benchmarking architectures against various constraints. Section 5 covers implementation of 3-D camera processor briefly. Concluding remark is given in Section 6 followed by reference in Section 7.

2 3-D CAMERA SYSTEM

A 3 Dimension camera system is based on Photon Mixer Device (PMD) [1][2][3][4] image sensor, which is used to capture distance information of 3-D Image. It works on time of flight (ToF) principle of IR light generated by the IR LED source, the radiation reflected off the target and captured by the image sensor. Furthest the object from the light source, minimum is the reflection on the image sensor. The 3-D PMD sensor data is processed by the Digital Signal Processor to generate three image parameters i.e., amplitude, offset and phase. These image parameters are sent to host computer system over USB communication. The image parameters are analyzed and reconstructed on host computer for 3-D object rendering.

The 3-D camera system is based on two main components, namely light emitter and light detector. The system block diagram in Fig-1 shows LED array driven by LED driver, which constitute the light emitter section. Rest of the blocks constitute the light detector, comprising of sub-blocks, namely PMD image sensor, Sensor analog output signal conditioner, ADC, Sensor time and control signal generator, Digital Signal Processing, Sensor data storage memory, USB device driver and controller. Besides these sub blocks the unit has lens and filter arrangement mounted on PMD sensor.

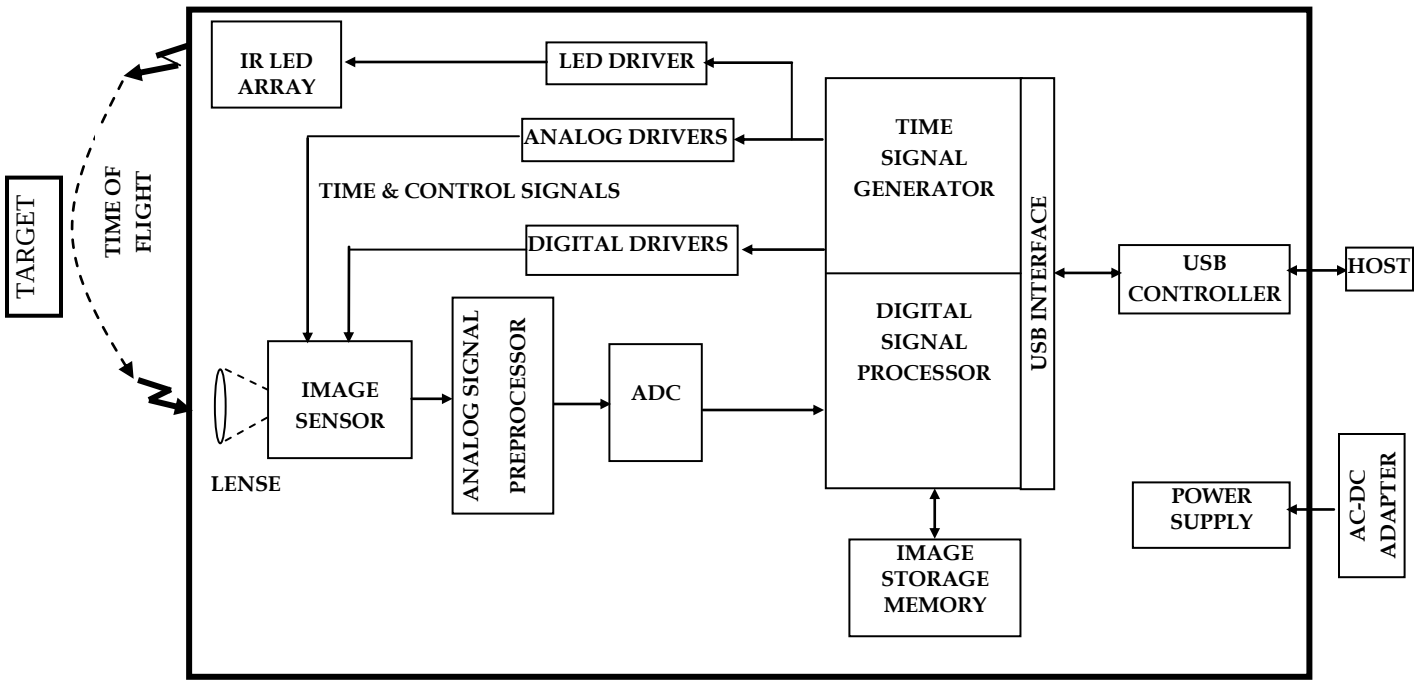

Fig-1 3-D camera system block diagram

The array of IR LED is driven by modulation signal, generated by the Time signal Generator (TSG). The PMD sensor captures IR reflected from the target object and converts to electrical signal. The electrical signal of PMD sensor is further conditioned and digitized by ADC and passed to the Digital signal Processor. The Digital Signal Processor process the ADC digitized PMD sensor data and transfer the processed 3-D image parameters like Amplitude, Offset, Phase to external host through high speed USB communication. Various low voltage supplies are generated on board powered by an AC-DC adapter connected to AC mains supply.

3 SYSTEM PARTITIONING

The 3-D camera system shown in Fig-1 can be partitioned into four major components listed here and shown in Fig-2.

1. Common electronics include LED array module with associated driver, PMD sensor signal conditioner, PMD time and control signal driver, Pre processing Noise filter of sensor data, Raw sensor data digitization by Dual channel ADC and power supply.

2. Storage of four frames sensor data in circular buffer in memory device.

3. Time and Signal Generator (TSG), Digital Signal processing (DSP) of the digitized sensor data and USB device driver.

4. Processed image data upload to the host by a USB communication.

ARCHITECTURE 1 - FPGA – Fig 3

The TSG, DSP and USB interface functionality can be implemented on a single FPGA. The external 256Kx16 bit SRAM device is used to implement a circular buffer and pixel processing of the continuous image stream from camera and then processed image is forwarded to external host system via USB communication. An external high speed USB controller device is used. Flash memory device is used to store the FPGA configuration data.

The FPGA can handle following functions.

1. Generation of Time and Control Signal for PMD image sensor and modulation signal for IR LED.

2. Interface to accept dual 16 bit ADC Data at 8 MHz sampling interval.

3. Low pass digital noise filter.

4. Memory interface logic to store result of filtered ADC input. Four image frames corresponding to 0^o, 90^o, 180^o, 270^o phase difference excited IR signal are stored at separate locations in memory. After capturing four frames data, each frame is retrieved and presented to pixel processing unit.

5. Pixel processing unit calculates phase shift, offset, and amplitude from four frame data. This unit is implemented using standard core of FPGA. These cores are Arctan, Multiplier, Divider and Adder.

6. USB interface to transfer the processed data to external USB controller.

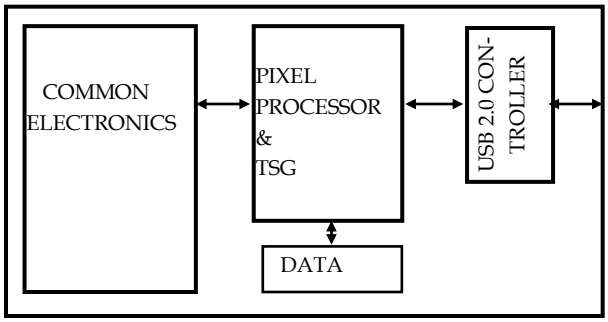

Figure-2 Top Level Design Architecture

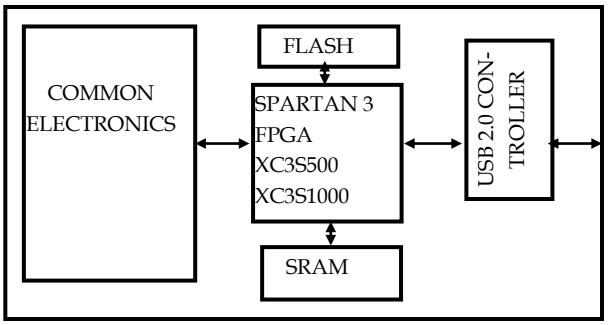

Figure 3 FPGA based architecture

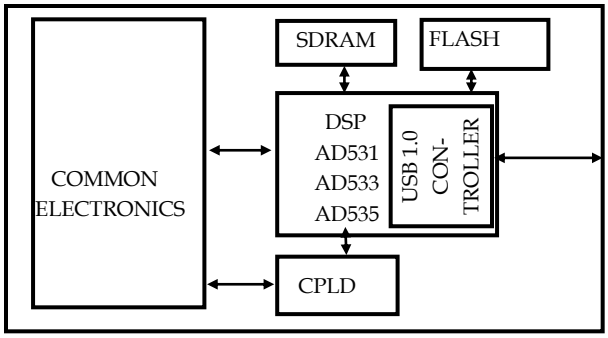

Figure 4 DSP and CPLD based architecture

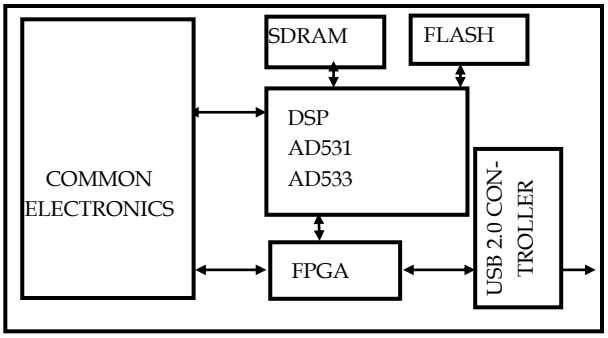

Figure 5 DSP and FPGA based architecture

ARCHITECTURE 2 – DSP - Fig 4

DSP functions can be implemented on a DSP device and the TSG function on a low cost CPLD device. The local DRAM memory connected to DSP device for program execution is used for storage of raw and processed image data. High end DSP device has built in USB controller.

The DSP processor can handle following functions.

1. Interface to accept dual 16 bit ADC Data at 8 MHz sampling interval.

2. Low pass noise filter.

3. Store result of filtered ADC input in memory. Four image frames corresponding to 0^o, 90^o, 180^o, 270^o delayed phase reflected IR signals would be stored at separate locations in memory. Then retrieve four frames data from memory and send to pixel image processing module.

4. Pixel processing module would calculate phase shift, offset, and amplitude from four frame data.

5. The processed data is stored temporarily and then transferred through DMA to USB.

The CPLD can handle:

6.TSG for PMD sensor and modulation signal generation for IR LED.

ARCHITECTURE 3 - DSP +FPGA - Fig 5

This Approach is DSP processor major and FPGA minor; as the DSP processor handles all compute intensive tasks and FPGA handles logic intensive functions.

The DSP processor can handle following functions.

1. Interface to accept dual 16 bit ADC Data at 8 MHz sampling interval.

2. Low pass FIR filters.

3. Store result of subtraction of filtered ADC input in memory. Four image frames corresponding to 0^o, 90^o, 180^o, 270^o delayed phase reflected IR signals would be stored at separate locations in memory. Then retrieve four frames data from memory and send to pixel image processing module.

4. Pixel processing module would calculate phase shift, offset, and amplitude from four frame data.

The FPGA can handle following functions.

5. The processed data is transferred through FPGA to external USB device.

6. TSG for PMD sensor and modulation signal generation for IR LED.

4 BENCHMARKING ARCHITECTURES

System tasks have been assigned to physical devices as explained in three identified architectures in section 3. Benchmark against design constraints cost, memory, size and power is shown in Table-1. The board size and power consumption are automatically reflected by the nos. of components and are obvious indicators of selection criteria.

The DSP processor selected was BlackFin from AMD[6], programmable logic devices Spartan3 FPGA and CoolRunner CPLD from Xilinx[5]. These vendors offer range of devices in terms of functionality and resources in same family. Other devices like USB controller, Memory, ADC are selected from established chip vendors. Microcontroller based USB controller (uC-USB) from Cypress offers easy integration and considered as an alternative to FPGA approach. Other miscellaneous components, PCB, power supply, passive components etc have been excluded for ease of comparison.

Design challenges are:

1) Uninterrupted buffer management of raw sensor data

2) Pixel processing of sensor data stored in circular buffer

3) USB device driver

4) Pre-design resource estimation and selection of right device.

5) Minimal risk and redundancy

6) Trial and error with new devices

ARCHITECTURE –1 – FPGA

In order to go ahead with minimal risk, three variants of the FPGA based architectures are envisaged, which require FPGA knowledgebase and the associated learning curves for implementation of USB device driver, pixel processing and appropriate FPGA device selection based on initial resource estimation.

ARCHITECTURE –2 – DSP

Knowing the limitation of DSP processor that there is no support logic for TSG functionality, a CPLD device is associated. The USB 1.0 functionality is available in higher model in the same Blackfin family, of course with a cost penalty.

ARCHITECTURE –3 – FPGA + DSP

This architecture was envisaged by the availability of sound knowledge base on DSP and with the conviction that the knowledge base on FPGA can be developed progressively as [project proceeds. A fallback on DSP in case of failure and risk of FPGA based design was a management decision looking at the time to market constraint.

SUMMARY OF BENCHMARK

Meeting the product performance at the sacrifice of cost and size was the prime factor for deciding the architecture. FPGA based architecture was finally selected overriding the risk of the learning curves in implementing circular buffer scheme, pixel processing and USB driver.

Table –1 Benchmark of Architectures

Design Platform	FPGA			DSP		DSP + FPGA		
Configuration	Small FPGA +uC-USB	Medium FPGA +uC-USB	Large FPGA + USB	Medium DSP + CPLD +uC-USB	Large DSP (USB) +CPLD	Small DSP + FPGA	Medium DSP + FPGA	Large DSP (USB) +FPGA
TSG done in	FPGA	FPGA	FPGA	CPLD	CPLD	FPGA	FPGA	FPGA
Pixel Processing	No	FPGA	FPGA	DSP	DSP	DSP	DSP	DSP
Mem. Interface	No	FPGA	FPGA	DSP	DSP	DSP	DSP	DSP
USB Interface	uC-USB	uC-USB	FPGA	uC-USB	AD535	FPGA	FPGA	AD535
ADC Interface	FPGA	FPGA	FPGA	CPLD	CPLD	FPGA	FPGA	FPGA
CPLD / FPGA	XC3S100 ($5)	XC3S500 ($18)	XC3S1000 ($24)	XC2C128-6 ($8)	XC2C128-6 ($8)	XC3S500 ($18)	XC3S500 ($18)	XC3S100 ($5)
DSP	No	No	No	ADSP-BF531 ($8)	ADSP-BF535 ($41)	ADSP-BF531 ($8)	ADSP-BF531 ($8)	ADSP-BF535 ($41)
SRAM 256Kx16	No	Yes ($4)	Yes ($4)	No	No	No	No	No
SDRAM 4MBX16	No	No	No	Yes ($6)	Yes ($6)	Yes ($6)	Yes ($6)	Yes ($6)
USB Controller	CY7C68013 ($13)	CY7C68013 ($13)	ISP1582 ($10)	CY7C68013 ($13)	-	ISP1582 ($10)	ISP1582 ($10)	-
ADC	AD9826 ($6.5)	AD9826 ($6.5)	AD9826 ($6.5)	AD9826 ($6.5)	AD9826 ($6.5)	AD9826 ($6.5)	AD9826 ($6.5)	AD9826 ($6.5)
Total Cost ($)	$24.5	$41.5	$44.5	$41.5	$61.5	$48.5	$48.5	$58.5
Board Space	Small	Medium	Large	Large	Medium	Large	Large	Large
Power reqd.	Small	Medium	Large	Large	Medium	Large	Large	Large
Issues	No Pixel proces	Cost	Size, Cost USB driver	Size, Cost	Cost USB speed	Size & cost USB driver	Size & cost USB driver	Size & cost USB speed
Trial & Error	Required	Required	Required	Nil	Nil	Required	Required	Required
Comments	Limited funcs	All functions	All functions	All functions	All functions	All functions	All functions	All functions

5 IMPLEMENTATION

The representative hardware of the 3-D camera processor is shown in Figure-6. The sensor used was PMD 19k [4] with 160x120 pixel resolution. Spartan3S1000 FPGA [5] was used to maximise percentage of function incorporation. The project was implemented; using Xilinx synthesis tools SE 7.2 SP4 [7], Xilinx ChipScope Debugging tool and Verification by Modelsim tool.

A brief explanation of the hardware is given here. The Timing signal generator inside FPGA generates appropriate signal as per the specification of PMD 19k sensor. Modulation outputs MOD_A and MOD_B from FPGA drive modulation inputs of the sensor through line drivers. Same modulations are given to LED driver. Video_a and Video_b are the output of the image sensor. These signals are scaled, amplified, filtered and then digitized by the dual channel 14-bit ADC. Digital outputs of ADCs are sampled by FPGA and filtered by a three-point FIR filter and stored in a SRAM.

The integration time, in other words, camera shutter time of the image sensor is user programmable and ranges from 1 ms to 4 ms. The integration and readout follows four phase shifting i.e at 0^o then 90^o, 180^o, 270^o as shown in Fig - 7. Four frames corresponding to 0^o, 90^o, 180^o, 270^o are stored at separate locations in SRAM.

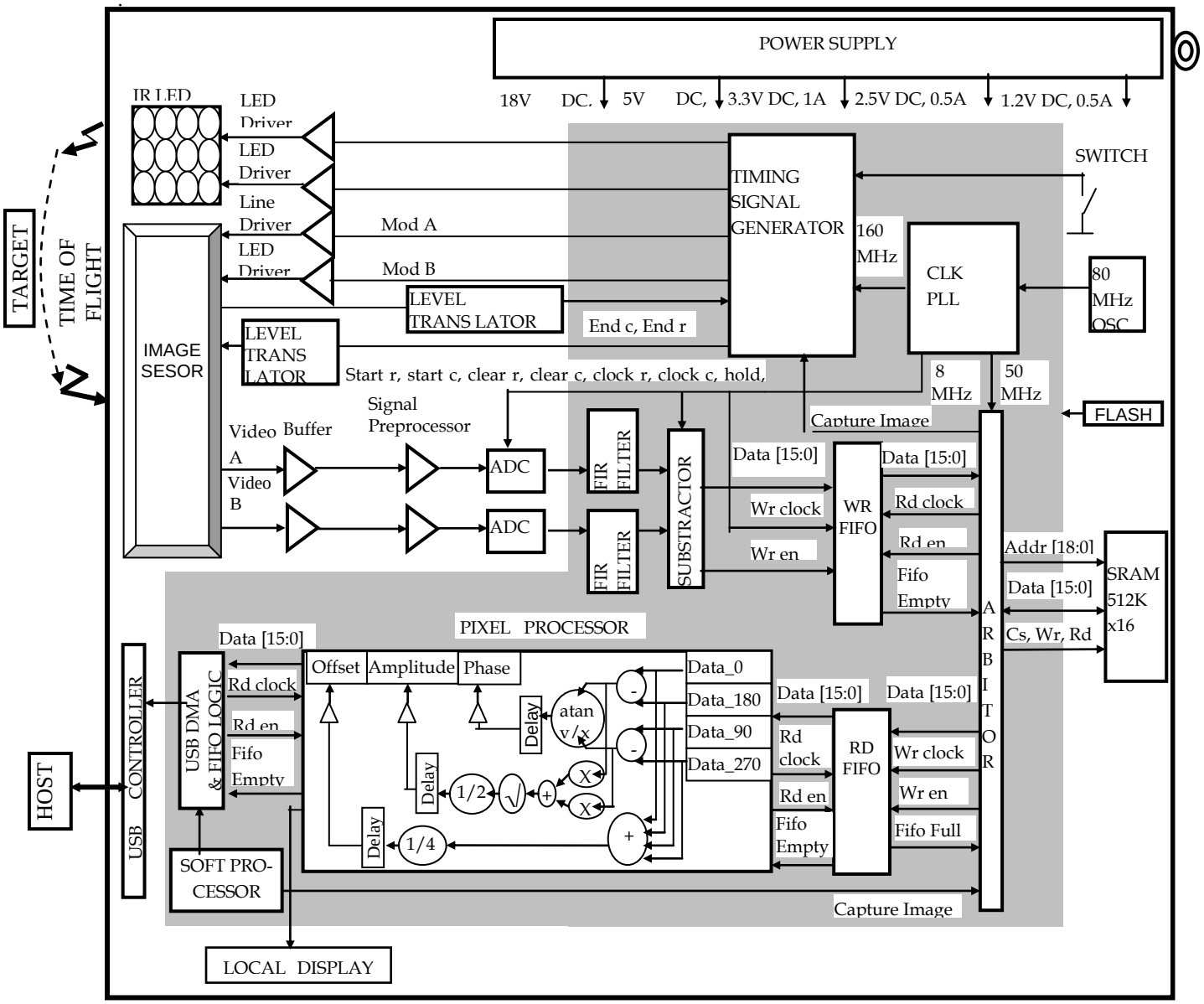

Figure 6 3-D Camera Processor

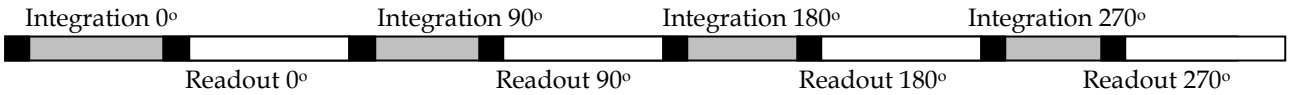

Figure 7 Camera integration and readout sequence

To increase USB frame rate ping-pong/circular buffering approach is used. In this approach SRAM is divided in to two blocks. Out of these two blocks one block is used to write incoming four frames where as reading of older four frames was carried out from other block. Read and write blocks are switched at every frame boundary.

After capturing four frames in SRAM, the sensor data is read and presented to pixel processing unit. Pixel processing unit calculates phase shift, offset, and amplitude based on following three equations.

$$\varphi = \arctan \frac{\Delta Uab(270^o) - \Delta Uab(90^o)}{\Delta Uab(0^o) - \Delta Uab(180^o)} \quad (1)$$

$$B = [\Delta Uab(270^o) + \Delta Uab(90^o) + \Delta Uab(0^o) + \Delta Uab(180^o)]/4 \quad (2)$$

$$A = [((\Delta Uab(270^o) - \Delta Uab(90^o))^2 + ((\Delta Uab(0^o) - \Delta Uab(180^o))^2]^{1/2} /2 \quad (3)$$

Where

φ = Phase shift

B = Offset

A = Amplitude

ΔUab = Difference of video_a and video_b

All above equations were implemented in FPGA in pixel processing unit. For implementing arc_tan function and square root function, Xilinx core CORDIC v3.0 was used. Phase correction logic was used to convert phase range +Π to -Π , into 0 to 2Π. Pipelining was done such that after some initial latency, first offset was written in FIFO, on next clock edge amplitude was stored in same FIFO, on next clock edge phase was stored in same FIFO. Thus for each pixel, offset, amplitude, phase information were stored consecutively in sequence in FIFO.

The Picoblaze soft processor embedded in FPGA overall controled major blocks i.e., timing signal generator, SRAM interface logic, pixel processing unit, USB interface.

A capture image signal generated by the soft processor triggered all the events in sequence thus achieving the synchronization among all blocks. It accessed the pixel processor FIFO to transfer the three image parameters to USB peripheral controller. At power-up it initialized the USB peripheral controller through USB interface logic. It read packets sent by host over USB and interpreted the request for sending calculated result of pixel processor. USB interface logic was responsible for transferring data to USB peripheral controller (ISP1582)[8] endpoint buffer.

The host calculated distance, reflectivity, and gray level based on the three image parameters i.e., offset, amplitude, phase and rendered the object for display.

6 Conclusion

Selection of the architecture for a 3-D camera SoPC design was done after benchmarking various design constraints. DSP on FPGA was exploited for signal processing of 3-D sensor image. The shaded section in Fig-7 included all digital logic and implemented in FPGA. Total cost of the standalone handheld prototype was approx. $50 plus the cost of the PMD sensor.

Future scope of the project can include rendering of the 3-D object locally on the target FPGA system using an embedded processor instead of the remote Host.

7 Reference

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